

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re patent application of:

Franco Motika, et al.

Serial No.: 10/780,878

Group Art Unit: 2138

Filing Date: February 19, 2004

Examiner: C. Tu

For: METHOD AND STRUCTURE FOR PICOSECOND-IMAGING-CIRCUIT-  
ANALYSIS BASED BUILT-IN-SELF-TEST DIAGNOSTIC

Honorable Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**SUBMISSION OF PRIOR ART**

Sir:

For the possible benefit of anyone subsequently evaluating the scope and/or validity of the above patent, it is respectfully requested that the following references cited in the corresponding Japanese Application, be placed in the file wrapper:

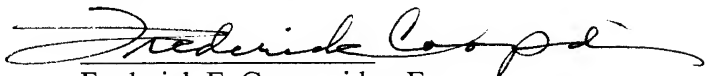
1. JP04192336A2 (Abstract only)
2. JP05304261A2 (Abstract only)

The undersigned has not reviewed the teachings of these references in detail and thus makes no representations concerning their relevancy or materiality.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to Assignee's Deposit Account No. 50-0510.

Respectfully submitted,



Frederick E. Cooperrider, Esq.  
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Date: April 7, 2008

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